|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **FUNCTIONAL SPECIFICATION** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |  |
| **Document Name** | | | | | | | | | | | | | | | | | | | **Document Number** | | | | | | | | | |
| **FPD Link: Link Implementation Specification** | | | | | | | | | | | | | | | | | | | **00.06.01.004** | | | | | | | | | |
|  | |  | |  | | |  | |  |  |  |  |  | |  |  |  |  | | |  | |  | |  |  |  |
|  | |  | |  | | |  | |  |  |  |  |  | |  |  |  |  | | |  | |  | |  |  |  |
|  | |  | |  | | |  | |  |  |  |  |  | |  |  |  |  | | |  | |  | |  |  |  |
|  | |  | |  | | |  | |  |  |  |  |  | |  |  |  |  | | |  | |  | |  |  |  |
|  | |  | |  | | |  | |  |  |  |  |  | |  |  |  |  | | |  | |  | |  |  |  |
| **DATE** | | |  | | **Ver** | **REVISIONS** | | | | | | | | | | | | | | **DR** | | **CK** | | **REFERENCE** | | | | |
| 4/24/2018 | | |  | |  | Draft | | | | | | | | | | | | | |  | |  | |  | | | | |
| 6/22/18 | | |  | | AA | Initial Release | | | | | | | | | | | | | |  | |  | | **MODIFIED BY** | | | | |
| 3/27/19 | | |  | | AB | Update to include FPD link IV chipsets | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | | **APPROVED BY** | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | |  | |  |  | | | | | | | | | | | | | |  | |  | |  | | | | |
|  | | | | | | |  | | | | | | (Previous editions may **NOT** be used) | | | | | | | | | | | | | | | | | |

# I. Scope

This document is a technical specification for a multiplexed FPD LINK III and IV network between automotive video ECU’s, an inter-systems network. In combination with a protocol standard for multiplex it is a full specification regarding communication, all requirements in the Technical Regulation for the specific ECU also have to be fulfilled.

This document shall be used to define and develop all production intent ECU’s using the TI FPD LINK III and IV Automotive Video Bus for the Ford Enterprise.

Attention: Failure to comply with these requirements of this specification by any production intent ECU may result in an inability to communicate on the vehicle network for which the ECU was intended.

## 1.1 Not in Scope

Requirements specifically related to the physical implementation of the FPD LINK III and IV network (e.g. Connectors, Wires, Physical Layer and other specifically related components) are not within the scope of this specification. Please see III. References

# II. Table of Contents

[I. Scope 2](#_Toc4766180)

[1.1 Not in Scope 2](#_Toc4766181)

[II. Table of Contents 3](#_Toc4766182)

[III. References 4](#_Toc4766183)

[1 Definitions/Abbreviations 4](#_Toc4766184)

[1.1 General Definitions 4](#_Toc4766185)

[1.2 Abbreviations used in this document 5](#_Toc4766186)

[2 PRODUCT OVERVIEW 6](#_Toc4766187)

[2.1 Automotive FPD Link III Example 6](#_Toc4766188)

[3 Implementation Requirements 6](#_Toc4766189)

[3.1 Type of Network (FPD Link) 6](#_Toc4766190)

[3.1.1 Maximum Clock Rate 6](#_Toc4766191)

[3.1.2 Forward Channel Data Rate 7](#_Toc4766192)

[3.1.3 Back Channel Data Rate 8](#_Toc4766193)

[3.1.4 Supported formats 8](#_Toc4766194)

[3.2 System Level 9](#_Toc4766195)

[3.2.1 FPD Link Network Topology 9](#_Toc4766196)

[3.2.2 Nodes and Links 10](#_Toc4766197)

[3.2.3 Common FPD Link Network Wakeup Source 10](#_Toc4766198)

[3.3 Local node requirements 10](#_Toc4766199)

[3.3.1 Local Node Initialization 10](#_Toc4766200)

[3.3.2 Local Node Status 14](#_Toc4766201)

[3.3.3 Local Node Error handling and recovery 16](#_Toc4766202)

[3.4 Specific Diagnostic Support via CAN 16](#_Toc4766203)

[3.4.1 FPD Link III Network Discovery at EOL/Service Bay 16](#_Toc4766204)

[3.4.2 FPD Link III Network Errors 17](#_Toc4766205)

[3.4.3 FPD Link III DTC reporting 17](#_Toc4766206)

[3.5 Remote Node Requirements 18](#_Toc4766207)

[3.5.1 Remote Node Initialization 18](#_Toc4766208)

[3.5.2 Remote Node Status 18](#_Toc4766209)

[3.5.3 Remote Node Error recovery 18](#_Toc4766210)

[4 VERIFICATION METHODS 18](#_Toc4766211)

[4.1 Node conformance tests 18](#_Toc4766212)

[4.2 Verification traceability 19](#_Toc4766213)

[Appendixes 21](#_Toc4766214)

[Appendix. 1 Approved FPD LINK Chipsets 21](#_Toc4766215)

[Appendix. 2 DTC/DID list 21](#_Toc4766216)

[Appendix. 3 Change log 21](#_Toc4766217)

# III. References

* The requirements of the documents listed in the following table, form a part of this specification. The revision levels shown in the table were the latest at the time this Functional Specification was written. In the event of a conflict between the requirements of this specification and these documents, the requirements of the documents in the table shall have precedence.

| **Rev Level** | **Requirement Document Name (ie, SDS/ARL requirements, Deviations, Engineering Specifications)** |
| --- | --- |
| AB | [1] - FPD LINK Physical Layer Specification 00.06.03.004 |
| AO or latest | [2] - Netcom Physical Layer Approved Components 00.06.03.002 |
|  | [3] - Feature – I2C over LVDS Communication Protocol [VDOC038838] |
|  | [4] - Texas Instruments Data sheets and user guides |
| AB | [5] - FPD Link Physical Layer Design Verification Checklist 00.06.03.401 |
|  | [6] - FPD Link Implementation Review Checklist 00.06.01.405 |
|  | [7] – TI datasheets1 |
|  | [8] – FPD LINK Cable/Connector Assembly Specification 00.06.01.005 |
|  | [9] - FPD LINK System Level Design Verification Checklist 00.06.01.404 |
|  |  |
|  |  |

Document References

1 Refer the Texas Instruments website (<http://www.ti.com/interface/fpd-link-serdes/products.html>) for the latest Data sheets, specific to the SerDes chipsets under consideration.

# Definitions/Abbreviations

## General Definitions

|  |  |
| --- | --- |
| Back Channel | Low speed data channel over which command and control data is sent |
| Bus | A bus is a collection of one or more wires connecting two or more nodes. Each electronic device (in this case: Host ECU, Master Node or Slave Node) is equipped with a specific, standardised electronic interface in order to guarantee compatibility between exchanged binary items of information |
| Deserializer | The deserializer converts FPD LINK III frames raw into video/display data |
| Display Processor | This is video data sink typically on the head unit or cluster or display module. It is connected to an FPD LINK III deserializer via I2C and high speed data lines. |
| Forward Channel | High speed data channel over which raw/uncompressed video data is sent |
| Host ECU | Electronic control unit that communicates on the CAN Network that uses FPD LINK III to send and receive data to peripheral devices |
| Host Microprocessor | Microprocessor unit that is part of the Host ECU that interfaces with the local node |
| Local Node | Local Node is attached to the main system processor and is responsible configuration and powermoding of the bus |
| Multiplex | To interleave or simultaneously transmit two or more messages/signals or sets of data on a single channel. |
| Network | A set of electronic and cabling devices facilitating the multidirectional exchange of information between two or more nodes on one or more busses. |
| Remote Node | Remote Node is attached to the Local node via FPD LINK III and it receives it’s configuration and powermoding from the local node over FPD LINK III |
| Sensor | This is a data source like camera imager, Lidar sensor etc. It is connected to an FPD LINK III serializer via I2C and high speed data lines. The sensor can be configured from FPD Link III from the back channel data. |
| Serializer | The serializer converts raw video/display data into FPD Link III frames and sends this over the data line at high bit rates |
| Pixel Clock | Product of image resolution frame rate colour depth and blanking interval |
| REF Clock | Driving FPD link when operating in sync mode |
| CSI-2 clock | Determines CSI data rate per lane |
| Ext clock mode | Clock driving serializer independent of deserializer clock |
| DVP clock | Special case of external clock for backward compatibility |
| Sync mode | Using single REF clock to drive both serializer and deserializer |
| CMLOUT | FPD link without backchannel used in dasy chain |
|  |  |
|  |  |

## Abbreviations used in this document

|  |  |
| --- | --- |
| BCC | Bi-Directional Control Channel |
| DID | Diagnostic Identifiers |
| DTC | Diagnostic Trouble Code |
| ECU | Electronic Control Unit |
| EMC | Electromagnetic Compatibility |
| FMC | Ford Motor Company |
| FPD LINK III | Flat Panel Display (FPD) Link III (TI Devices Trademark) |
| FPD LINK IV | Flat Panel Display (FPD) Link IV (TI Devices Trademark) – next gen |
| FPS | Frames Per Second |
| HLSL | High Level Hardware and Software Link |
| ISO | International Standards Organisation |
| LVDS | Low Voltage Differential Signalling |
| PCB | Printed Circuit Board |
| PDB | Power Down Mode Pin |
| POC | Power Over Coax |
| PoDL | Power over Data Line (same as in POC) |
| SERDES | Serializer-Deserializer |
| TI | Texas Instruments |
| STP | Shielded Twisted Pair |
| CMLOUT | Current mode logic output |
|  |  |

# PRODUCT OVERVIEW

The specification addresses the implementation of the TI Automotive Video network.

## Automotive FPD Link III Example



Figure 2.1.1: FPD LINK Example

# Implementation Requirements

This document specifies the High Level Hardware and Software Link (HLSL) requirements related to the implementation of a TI FPD LINK III and IV bus network.

The term FPD LINK is used here after to refer to both FPD LINK III and IV bus networks unless otherwise specified.

The FPD Link is a point to point link capable of sending video and control data or display data across a COAX or Shielded twisted Pair cable or shielded parallel pair.

In the above example, the remote node (Serializer) is connected to an image sensor that is the source of video data, this video data is then transmitted by the remote node using FPD Link to the local node (DeSerializer). The remote node is capable of being controlled and configured by the low speed back channel of the link. The local node is responsible for power moding and configuration of the link through the low speed bi-directional control channel (BCC).

In other applications such as infotainment systems, the local node will contain the serializer that interfaces with the head unit and will send display data using FPD Link to the remote node that will contain the deserializer that interfaces with a display.

## Type of Network (FPD Link)

### Maximum Clock Rate

DL\_FPD LINK\_REQ\_\_

Applications shall not exceed highest achievable pixel clock or CSI clock for DPHY.

|  |  |  |  |
| --- | --- | --- | --- |
| **Chipsets** | **Max Pixel Clock** | **Max REF Clock** | **CSI-2 clock frequency2** |
| (MHz) | (MHz) | (MHz) |
| DS90UB91-3A/4A | 100 | N/A | N/A |
| DS90UH927/8 | 85 | N/A | N/A |
| DS90UB933/4 | 100 | N/A | N/A |
| DS90UH947/8 Single lane | 96 | N/A | N/A |
| DS90UH947/8 Dual lane | 170 | N/A | N/A |
| DS90UB953 | N/A | 26 | 416 |
| DS90UB954 | N/A | 26 | 832 |
| DS90UB960 | N/A | 26 | 832 |
| DS90UB971 | N/A | 25 | 1250 |
| DS90UB972 | N/A | 25 | 1250 |
| DS90UB9702 | N/A | 25 | 1250 |

Table 1: Maximum Clock Rate

**2** The high speed data bit rate per lane is 2 x CSI clock frequency

The product of H, V, FPS, Blanking factor and bits per color shall not exceed the maximum achievable bit rate by each SerDes.

Example: For DS90UB927/8 -1920(H) x 720(V) x 60(FPS) x 24(color) <= 2975 Mbps (highest achievable bit rate for DS90UB927/8).

When using multiple chipsets, the chipset with lower data rate/pixel clock takes precedence.

Examples:

Display applications:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Chipsets** | **Standard** | **H** | **V** | **fps** | **Color** | **Blanking Factor** | **Raw video rate** | **Pixel Clock** |
| (Lines) | (Lines) | (Hz) | (bpp) | (%) | (Mbps) | (MHz) |
| DS90UB927/8 | 720p | 1280 | 720 | 60 | 24 | 110 | 1460 | 61 |
| DS90UH947/8 | 1080p | 1920 | 1080 | 60 | 24 | 110 | 3285 | 137 |
| DS90UH947/8 | 1080p  (WUXGA) | 1920 | 1200 | 60 | 24 | 110 | 3650 | 152 |

Camera applications (DVP based):

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Chipsets** | **Standard** | **H** | **V** | **fps** | **Color** | **Blanking Factor** | **Raw video rate** | **Pixel Clock** |
| (Lines) | (Lines) | (Hz) | (bpp) | (%) | (Mbps) | (MHz) |
| DS90UB913A/14A | 1MP | 1280 | 800 | 30 | 24 | 110 | 811 | 75 |
| DS90UB933/34 | 1.4MP | 1280 | 1080 | 30 | 24 | 110 | 1095 | 83 |

Camera applications (MIPI CSI based):

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Chipsets** | **Standard** | **H** | **V** | **fps** | **Color** | **Protocol and Blanking Overhead** | **Maximum CSI Input Rate** |
| (Lines) | (Lines) | (Hz) | (bpp) | (%) | (Mbps) |
| DS90UB953/54 | 2MP | 1920 | 1080 | 60 | 20 | 125 | 3328 |
| DS90UB971 | 8MP | 3840 | 2160 | 40 | 20 | 103 | 8252 |
| DS90UB972 | 8MP | 3840 | 2160 | 40 | 20 | 103 | 8252 |
| DS90UB9702 | 8MP | 3840 | 2160 | 40 | 20 | 103 | 8252 |

Note: The image sensor and MIPI CSI-2 lines (if applicable) can add up to ~20% of extra overhead on top of the above mentioned protocol overhead.

Table 2: Examples of Camera and Display applications

### Forward Channel Data Rate

DL\_FPD LINK\_REQ\_\_

Applications shall not exceed highest achievable forward channel data rate

DL\_FPD LINK\_REQ\_\_

Applications shall use appropriate cable/connectors assemblies based on channel frequency range for forward and back channel. Refer to [8] for more details.

|  |  |  |
| --- | --- | --- |
| **Chipsets** | **Forward channel max data rate** | **Forward Channel freq range** |
| DS90UB913A/14A | 10-bit mode: 1400 Mbps  12-bit mode: 1400 Mbps | 350 - 700 MHz  350 - 700 MHz |
| DS90UB933/34 | 10-bit mode: 1400 Mbps  12-bit mode: 1867 Mbps | 350 - 700 MHz  350 - 934 MHz |
| DS90UB953/54 | Sync mode: 4160 Mbps  Ext clock mode: 4160 Mbps | 920 - 2080 MHz  1000 - 2080 MHz |
| DS90UB927/8 | 2975 Mbps | 263 - 1488 MHz |
| DS90UH947/8 | Single lane: 3360 Mbps  Dual lane: 2975 Mbps (per lane) | 438 - 1680 MHz  438 - 1488 MHz |
| DS90UB960 | Sync mode: 4160 Mbps  (up to 4 lanes)  Ext clock mode: 4160 Mbps | 920 - 2080 MHz  1000 - 2080 MHz |
| DS90UB971/2 | Sync Mode: 8500 Mbps  (upto 4 lanes) | 2080 - 4250 MHz |
| DS90UB9702 | Sync Mode: 8500 Mbps  (upto 4 lanes) | 2080 - 4250 MHz |

Table 3: Forward Channel Data Rate

### Back Channel Data Rate

DL\_FPD LINK\_REQ\_\_

Applications shall not exceed highest achievable back channel data rate

|  |  |  |  |
| --- | --- | --- | --- |
| **SerDes Chip Pair** | **Back channel data rate** | **Back channel freq range** | |
| **Minimum (MHz)** | **Maximum (MHz)** |
| DS90UB913A/14A | 2.5 Mbps | 1 | 3 |
| DS90UB933/34 | 2.5 Mbps | 1 | 3 |
| DS90UB953/54 | 50 Mbps (Sync clock) | 25 | 50 |
| 25 Mbps (Sync clock, ½ rate) | 12.5 | 25 |
| 10 Mbps (Async) | 5 | 10 |
| 2.5 Mbps (DVP clock) | 1 | 3 |
| DS90UB927/8 | 10 Mbps | 4 | 12 |
| DS90UH947/8 | 20 Mbps | 8 | 24 |
| DS90UB960 | 50 Mbps (Sync clock) | 25 | 50 |
| 25 Mbps (Sync clock, ½ rate) | 12.5 | 25 |
| 10 Mbps (Async) | 5 | 10 |
| 2.5 Mbps (DVP clock) | 1 | 3 |
| DS90UB971/72/702 | 100 Mbps (Sync Clock) | 50 | 100 |
| 10 Mbps (Async) | 5 | 10 |

Table 4: Back Channel Data Rate

### Supported formats

DL\_FPD LINK\_REQ\_\_3.1.4.1

Applications shall use only supported format by respective chipsets.

|  |  |  |
| --- | --- | --- |
| **Video format provided to serializer** | **Supported by UB936, UB954, UB96x, UB97x** | **CSI data type on Deserializer** |
| YCbCr\_422\_8\_8 | Yes | Native CSI YUV422 8-bit |
| YCbCr\_422\_10\_10 | Yes | Native CSI YUV422 10-bit |
| CCIR656 (BT.656) | No | N/A |
| RGB888\_12\_12 | Yes | Native RGB888 |
| RGB565\_8\_8 | Yes | Native RGB565 |

Table 5: Supported formats

## System Level

### FPD Link Network Topology

The automotive video bus link consists of one shielded twisted pair (STP) or COAX wire cables running from one/multiple local nodes to one/multiple remote nodes. See figure 2.1 Automotive FPD Link III Network Example for point-to-point topology, see Fig 3.1 for multi port de-serializer hub and see Fig 3.2 for single point to multiport serializer topology.



Fig 3.2.1: Multi-port De-serializer hub



Fig 3.2.2: Multiport Serializer



Fig 3.2.3: FPD Link IV CMLOUT daisy-chain topology

### Nodes and Links

Each link is a point to point network consisting of one Serializer Tx port and one Deserializer Rx port. Several ports can be combined in a single Serializer or De-serializer chip.

FPD Link IV supports CMLOUT that allows daisy-chaining between SerDes devices to transfer sensor data to multiple off-board processors.

### Common FPD Link Network Wakeup Source

DL\_FPD LINK\_REQ\_\_

The local node shall receive vehicle powermodes from the host ECU via CAN. FPD LINK high level powermoding will be the responsibility of the local node (can be Serializer or Deserializer).

The local node is responsible for initialization of the link during power up and may be responsible for providing full operational power to the remote node.

The local node must have the ability to cycle power to the Serializer/Deserializer IC in the remote node. This could be done using the POC feature of FPD Link or some remote method (CAN link).

## Local node requirements

The FPD LINK network consists of one local node, one or more remote nodes, and one or more peripheral devices attached to a remote node. The Local node communicates to the host microprocessor and one or more downstream remote nodes. The local node initiates all communication to/from the remote node and peripheral devices.

### Local Node Initialization

DL\_FPD LINK\_REQ\_\_

Each device requires specific initialization information. This will be performed through the local node by reading and writing specific “registers”.

This information shall be passed from the host microprocessor to the local node, then from the local node to one or more remote nodes at startup/EOL.

The remote peripheral node can be pre-configured with all information with no host microprocessor interaction needed with the approval from Advanced Netcom Team

Table 6a and 6b (below) contains registers in the chipsets that shall have values written to or verified during initialization. Values are to be determined from the appropriate data sheets and based on the system use case of the chipsets.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. Local node setup: | | | | | | | | | |
| **Description** | **Register addresses** | | | | | | | | |
|  | **UB**  **913A** | **UB**  **914A** | **UB**  **933** | **UB**  **934** | **UB**  **953** | **UB**  **954/**  **960** | **UH**  **927/**  **947** | **UH**  **928** | **UH**  **948** |
| I2C Device Address | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 |
| FPD Device ID | N/A | N/A | N/A | 0xF0- 0xF5 | 0xF0- 0xF5 | 0xF0- 0xF5 | 0xF0- 0xF5 | 0xF0- 0xF5 | 0xF0- 0xF5 |
| Set bit mapping | N/A | 0x1F | N/A | 0x6D | N/A | 0x6D | 0x04 | 0x49 | 0x49 |
| Set repeater mode | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | 0x23 |
| Set cable type | N/A | N/A | N/A | 0x6D | N/A | 0x6D | N/A | N/A | 0x23 |
| Set clock source | 0x35 | N/A | 0x35 | N/A | 0x05, 0x06, 0x07 | 0x58 | 0x03 | 0x02 | 0x02 |
| Set local CSI interface | N/A | N/A | N/A | N/A | 0x02, 0x20 | 0x1F, 0x21, 0x33, 0x34, 0x4B, 0x6D | N/A | N/A | N/A |
| Set data path & ports | 0x05 | 0x1F | 0x05 | 0x02, 0x25, 0x3B, 0x4C | 0x03 | 0x0C, 0x20, 0x59 | 0x12, 0xC0 | 0x02, 0x22, 0x23 | 0x02, 0x22, 0x23 |
| HDCP control | N/A | N/A | N/A | N/A | N/A | N/A | 0xC2, 0xC3, 0xC4 | 0xC0, 0xC1, 0xC4 | 0xC0, 0xC1, 0xC4 |
| Set GPIO | 0x0D, 0x0E | 0x1D, 0x1E | 0x0D, 0x0E | 0x0D, 0x0E, 0x0F, 0x10, 0x11, 0x12, 0x13, 0x18 | 0x0D, 0x0E | 0x0F, 0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x18 | 0x0D, 0x0E, 0x0F, 0x10, 0x11 | 0x1D, 0x1E, 0x1F, 0x20, 0x21 | 0x1D, 0x1E, 0x1F, 0x20, 0x21 |
| 1. Configuring I2C for remote communication: | | | | | | | | | |
|  | **UB**  **913A** | **UB**  **914A** | **UB**  **933** | **UB**  **934** | **UB**  **953** | **UB**  **954/**  **960** | **UH**  **927/**  **947** | **UH**  **928** | **UH**  **948** |
| Enable I2C pass-through | 0x03 | 0x03 | 0x03 | 0x58 | 0x32 | 0x58 | 0x03 | 0x03 | 0x03 |
| Set Slave ID | 0x08 | 0x08 | 0x08 | 0x5D | 0x39 | 0x5D | 0x07 | 0x08 | 0x08 |
| Set Slave Alias | 0x09 | 0x10 | 0x09 | 0x65 | 0x41 | 0x65 | 0x08 | 0x10 | 0x10 |
| Set SCL High/Low Times | 0x11, 0x12 | 0x40, 0x41 | 0x11, 0x12 | 0x0A, 0x0B | 0x0B, 0x0C | 0x0A, 0x0B | 0x18, 0x19 | 0x26, 0x27 | 0x26, 0x27 |
| 1. Checking link status: | | | | | | | | | |
|  | **UB**  **913A** | **UB**  **914A** | **UB**  **933** | **UB**  **934** | **UB**  **953** | **UB**  **954/**  **960** | **UH**  **927/**  **947** | **UH**  **928** | **UH**  **948** |
| Read back partner I2C addr (local) | 0x06 | 0x06 | 0x06 | 0x5B | 0x37 | 0x5B | 0x06 | 0x07 | 0x07 |
| Detect Valid Clock | 0x0C | 0x1C | 0x0C | 0x4E, 0x4F, 0x50, | 0x52 | 0x04, 0x4E, 0x4F, 0x50, 0xA5 | 0x0C | 0x1C | 0x1C |
| Detect Link/Lock | 0x0C | 0x1C | 0x0C | 0x04, 0x4D | 0x52 | 0x04, 0x4D | 0x0C | 0x1C | 0x1C |
| 1. Verify if lock is achieved using register above | | | | | | | | | |
| 1. Clear errors and error count only if lock was achieved in previous step (4) | | | | | | | | | |
| 1. Verify remote configuration across link, read back all remote partner in table above I2C registers and update if required | | | | | | | | | |

Table 6a: Local Node Initialization for FPD Link III chipsets

|  |  |  |  |
| --- | --- | --- | --- |
| 1. Local node setup: | | | |
| **Description** | **Register addresses** | | |
|  | **UB971** | **UB972** | **UB9702** |
| I2C Device Address | 0x00 | 0x00 | 0x00 |
| FPD Device ID | 0xF0-0xF5 | 0xF0-0xF5 | 0xF0-0xF6 |
| Set bit mapping | N/A | N/A | N/A |
| Set repeater mode | N/A | N/A | N/A |
| Set cable type | N/A | N/A | N/A |
| Set clock source | N/A | N/A | N/A |
| Set local CSI interface | 0x02, 0x20 | 0x1F, 0x21, 0x33, 0x34, 0x4B, 0x6D | 0x1F, 0x21, 0x33, 0x34, 0x4B, 0x6D |
| Set data path & ports | 0x03 | 0x0C, 0x20, 0x59 | 0x0C, 0x20, 0x59 |
| HDCP control | N/A | N/A | N/A |
| Set GPIO | 0x0D, 0x0E | 0x0F, 0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x18 | 0x0F, 0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, 0x18 |
| 1. Configuring I2C for remote communication: | | | |
|  | **UB971** | **UB972** | **UB9702** |
| Enable I2C pass-through | 0x32 | 0x58 | 0x58 |
| Set Slave ID | 0x39 | 0x5D | 0x5D |
| Set Slave Alias | 0x41 | 0x65 | 0x65 |
| Set SCL High/Low Times | 0x0B, 0x0C | 0x0A, 0x0B | 0x0A, 0x0B |
| 1. Checking link status: | | | |
|  | **UB971** | **UB972** | **UB9702** |
| Read back partner I2C addr (local) | 0x37 | 0x5B | 0x5B |
| Detect Valid Clock | 0x52 | 0x04, 0x4E, 0x4F, 0x50, 0xA5 | 0x4E, 0x4F, 0x50, 0x3D |
| Detect Link/Lock | 0x52 | 0x04, 0x4D | 0x4D |
| 1. Verify if lock is achieved using register above | | | |
| 1. Clear errors and error count only if lock was achieved in previous step (4) | | | |
| 1. Verify remote configuration across link, read back all remote partner in table above I2C registers and update if required | | | |

Table 6b: Local Node Initialization for FPD Link IV chipsets

Chipset power-up sequence

DL\_FPD LINK\_REQ\_\_

Power-Up sequencing and PDB Pin setup must comply with instructions provided in the appropriate datasheets [7].

Initialization Time

DL\_FPD LINK\_REQ\_\_

The host microprocessor shall be capable of completing initialization of the FPD LINK network (1 Local node, and up to 6 remote nodes) within 350ms of a wakeup event.

The FPD LINK system may be configured at vehicle runtime IF it can be completed within350ms,otherwise the FPD LINK system shall be configured at EOL/Service Bay and stored in non-volatile memory.

Video master clock

DL\_FPD LINK\_REQ\_\_

The host microprocessor shall support supplying the Video Master Clock to the Master FPD LINK chip (Local node) within 50ms of power up. This clock stream is required even if the video system is not on or functional. The application of the clock with respect to the power rails must meet data sheet specifications.

Software Driver

DL\_FPD LINK\_REQ\_\_

The host microprocessor shall utilize an approved FPD LINK software driver to communicate to/from the FPD LINK local node. This software shall be derived from TI recommended porting and shall be reviewed/approved by the EESE video section.

The driver shall support I2C communication with the host microprocessor to support functions such as initialization, status monitoring, interrupts, diagnostics and error recovery.

I2C Clock Stretching

DL\_FPD LINK\_REQ\_\_

Host microprocessor acting as an I2C master shall support clock stretching for I2C communication with Local node.

GPIO state during loss of lock

DL\_FPD LINK\_REQ\_\_

No GPIO pins including INTB shall be driven (will remain in a safe state) that are linked to the remote node during a loss of lock event.

Disabling unused channels on hubs

DL\_FPD LINK\_REQ\_\_

Any unused channel in a multi port chipset shall be disabled by writing to appropriate registers in sequence.

Example for disabling a port on UB 960

1. Select unused ports of the deserializer using register 0x4C.

2. Set bits [7:4] of the register 0x58 in the deserializer to “0”.

### Local Node Status

The FPD LINK network host microprocessor shall be capable of determining FPD LINK network errors on the local node, or any of its remote nodes and peripherals. The Host ECU shall set an FPD LINK Network Specific Diagnostic DTC, and an additional code identifying the specific node and/or type of error. List of DTC’s/DID’s are listed in appendix 2.

Auto equalization behavior

DL\_FPD LINK\_REQ\_\_

The LVDS chipset has an auto equalization (AEQ) behavior. When attempting to establish an LVDS link, the deserializer will begin with the minimum EQ setting and try to lock. If unsuccessful, it increments EQ and tries again. It repeats this routine until lock is established. Resetting the local node forces a restart at the beginning of the algorithm.

In any situation where local node is powered and running the search algorithm before the remote node is ready, the EQ setting could lock to a larger-than-necessary value.

Therefore, the host microprocessor shall reset the local node only after resetting the remote node.

The chipset should arrive in a stable lock condition within 50mS after reset.

Loss of Lock Fault

DL\_FPD LINK\_REQ\_\_

The host ECU shall have the ability to monitor Lock status using the lock status bit in the appropriate register (see table 7).

This status shall be reported via DID “Loss of Lock Fault” if the local node reports a loss-of-lock event.

The host microprocessor shall implement a counter and have the ability to set DTC “Loss of Lock” if there are greater than 5 loss-of-lock events during any single ignition cycle. This will indicate a signal-quality problem with communication. Deserializer lock indicator output pin can also be monitored using digital input line to the microcontroller.

Detection and reporting of FPD LINK III network errors

DL\_FPD LINK\_REQ\_\_

The FPD LINK local node shall support detection and reporting of the following FPD LINK network errors:

1. Errors during local node FPD LINK Network Configuration:

If the local node detects errors that result in a no configuration condition the host microprocessor shall have the ability to report DTC “Unable to configure FPD link” for this condition. The host microprocessor shall monitor registers in table 7a and 7b for this condition.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Description** | **Register Addresses** | | | | | | | |
| **UB**  **913A/**  **933** | **UB**  **914A** | **UB**  **934** | **UB**  **953** | **UB**  **954/**  **960** | **UH**  **927/**  **947** | **UH**  **928** | **UH**  **948** |
| Detect Valid Clock | 0x0C | 0x1C | 0x4E, 0x4F, 0x50 | 0x52 | 0x04, 0x4E, 0x4F, 0x50, 0xA5 | 0x0C | 0x1B, 0x1C | 0x1C |
| Detect Lock | 0x0C | 0x1C | 0x04, 0x4C, 0x4D | 0x52 | 0x04, 0x4C, 0x4D | 0x0C | 0x1C | 0x1C |

Table 7a: Clock and Lock registers for FPD Link III chipsets

|  |  |  |  |
| --- | --- | --- | --- |
| **Description** | **Register Addresses** | | |
| **UB971** | **UB972** | **UB9702** |
| Detect Valid Clock | 0x52 | 0x04, 0x4E, 0x4F, 0x50, 0xA5 | 0x4E, 0x4F, 0x50, 0x3D |
| Detect Lock | 0x52 | 0x04, 0x4D | 0x4D |

Table 7b: Clock and Lock registers for FPD Link IV chipsets

1. Network Errors counts during operation of the FPD LINK network (w/ Non-volatile DID support):

These error counters will determine channel data integrity by reporting of CRC and parity errors.

The host microprocessor shall have the ability to monitor these error counts by polling or monitoring registers specified in table 8a and 8b.

The error counts can be reported via DID “Network Error“

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Description** | **Register Addresses** | | | | | | | | |
| **UB**  **913A/933** | **UB**  **914A** | **UB**  **934** | **UB**  **953** | **UB**  **954** | **UB**  **960** | **UH**  **927/**  **947** | **UH**  **928** | **UH**  **948** |
| Back channel data integrity | 0x0A, 0x0B | NA | NA | 0x55, 0x56 | NA | 0x47 | 0x0A, 0x0B, | NA | NA |
| Forward channel data integrity | NA | 0x1A, 0x1B | 0x4E, 0x55, 0x56 | NA | 0x55,  0x56 | 0x55, 0x56 | NA | 0x06 | 0x41 |

Table 8a: Errors counter registers for FPD Link III chipsets

|  |  |  |  |
| --- | --- | --- | --- |
| **Description** | **Register Addresses** | | |
| **UB971** | **UB972** | **UB9702** |
| Back channel data integrity | 0x55, 0x56 | NA | NA |
| Forward channel data integrity | NA | 0x55,  0x56 | 0x55,  0x56 |

Table 8a: Errors counter registers for FPD Link IV chipsets

1. Transient Errors during operation of the FPD LINK III network (w/ Non-volatile DID support):

These are errors that occur during operation that include link, CRC, parity, forward channel sequence. Any transition in values during normal operation indicates an error event has occurred.

The host microprocessor shall have the ability to monitor these error events by polling error flag registers specified in table 9a and 9b.

These errors can be reported via DID “Transient Error“

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Description** | **Register Addresses** | | | | | | | | |
| **UB**  **913A/933** | **UB**  **914A** | **UB**  **934/**  **954** | **UB**  **953** | **UB**  **960** | **UH**  **927** | **UH**  **928** | **UH**  **947** | **UH**  **948** |
| Error flag | 0x0C | 0x1C | 0x4D | 0x52 | 0x4D,  0x4E | 0x0C | 0x06,  0x1C | 0x0C | 0x06 |
| Soft reset | 0x01 | 0x01 | 0x01 | 0x01 | 0x01 | 0x01 | 0x01 | **0x013** | 0x01 |

Table 9: Transient error registers for FPD Link III chipsets

**3 Not** valid for I2C voltage below 1.8v should use PDB instead

|  |  |  |  |
| --- | --- | --- | --- |
| **Description** | **Register Addresses** | | |
| **UB971** | **UB972** | **UB9702** |
| Error flag | 0x52 | 0x4D,  0x4E | 0x4D,  0x4E |
| Soft reset | 0x01 | 0x01 | 0x01 |

Table 9b: Transient error registers for FPD Link IV chipsets

### Local Node Error handling and recovery

Error handling procedure

DL\_FPD LINK\_REQ\_\_

The FPD LINK network host ECU shall support the following error handling procedures:

1. For hard network errors (errors which require one or more Local or remote nodes to be re-initialized) which occur at a normal FPD LINK wakeup event and require re-initialization of the FPD LINK network, the host microprocessor shall first attempt a soft rest using the soft reset register specified in Table 9a and 9b. If unsuccessful, then the host microprocessor shall attempt a controlled power shutdown, re-enable power to the local node and perform normal re-initialization sequence. The chipsets will need to be reinitialized according to REQ\_\_3.2.1.1.The host microprocessor shall perform constant retries (reset and bring up) until the FPD LINK network starts, or the wakeup source is turned off unless it’s determined that reset procedure cannot recover the device.
2. For transient errors (detected by the local node, or detected by the remote nodes) which occur after a successful key on or other startup event, the host microprocessor shall attempt a soft rest using the reset register.

Remote node being unresponsive/offline

DL\_FPD LINK\_REQ\_\_

During normal operation, if the local node detects a condition where the remote node has become non-functional, either Link Detect Fault or Loss of Communication, the host microprocessor shall perform a full power-cycle as an attempt to recover the remote node. A full power cycle includes a controlled power shutdown, re-enabling power to the local node and performing a normal re-initialization sequence. The host microprocessor shall monitor appropriate registers specified in REQ\_\_3.2.2.3 to determine fault condition.

In case the host ECU isn’t directly responsible for supplying power to the remote node an alternate method can be used to remove power from the remote node after approval from Advance Netcom.

## Specific Diagnostic Support via CAN

### FPD Link III Network Discovery at EOL/Service Bay

DL\_FPD LINK\_REQ\_\_

The FPD LINK Host ECU shall support a Diagnostic Routine that supports FPD LINK network initialization, remote node discovery and writing the correct configuration information to the local node and remote nodes. The routine shall support a command to set the correct configuration, and shall return an appropriate success/failure code. The FPD LINK system may be configured at vehicle runtime without a diagnostic routine if it can be completed within 350ms.

The host microprocessor shall have the ability to determine if the local node has a general electric failure and shall set DTC “LVDS General Electric Failure” for this error.

### FPD Link III Network Errors

DL\_FPD LINK\_REQ\_\_

If the FPD LINK III network fails to initialize after a wakeup event, the Host ECU shall support one or more Diagnostic Trouble Codes (DTC), and Data Identifier (DID) counters indicating the number of specific errors via the CAN network. The specifics for determining DTC and DID counters have been specified in REQ\_\_3.3.2.3.

### 3.4.3 FPD Link III DTC reporting

Link Status

DL\_FPD LINK\_REQ\_\_3.4.3.1

When the Host ECU is providing power to the local node, the host microprocessor shall monitor link and clock using the appropriate status register specified in Table 7a and 7b. The host microprocessor shall have the ability to detect loss of link and shall be reported via DID “LVDS Link Fault”

The host ECU shall set DTC “LVDS Link Fault” based on this error. This will indicate a connection fault.

Lock Status

DL\_FPD LINK\_REQ\_\_3.4.3.2

The host microprocessor shall monitor the LOCK Pin or LOCK status change register if available for any loss-of-lock and shall have the ability to set DID “Loss of Lock” if the local node reports a loss-of-lock event.

The host microprocessor shall implement a counter and have the ability to set DTC “Loss of Lock” if there are greater than 5 loss-of-lock events during any single ignition cycle. This will indicate a signal-quality problem with communication to the remote node.

Unexpected Reset

DL\_FPD LINK\_REQ\_\_3.4.3.3

The local node register LOCK\_STS is set (=1) when lock is achieved. Any transition from 1 -> 0 during normal operation indicates an unexpected reset.

The host microprocessor shall have the ability to monitor this register and record this event,

This event can be reported via DID “Unexpected Reset” if an unexpected reset was detected.

The host microprocessor shall implement a counter and have the ability to record this event.

This event can be reported via DTC “Unexpected Reset” if there are greater than 5 events detected during any single ignition cycle.

Peripheral device reset request

DL\_FPD LINK\_REQ\_\_3.4.3.4

The peripheral devices connected to a local/remote node are permitted to request a full power-cycle. These devices usually make this request after detecting loss-of-lock, low-voltage dropout, and backlight fault. The host microprocessor shall comply with this request only if the fault can be fixed by soft reset or cycling power.

The host microprocessor shall first attempt a soft rest using the reset register and then perform a controlled power shutdown, re-enable power to the local node and perform a normal re-initialization sequence.

The host microprocessor shall keep track of these reset requests and have the ability to record this event. The hose ECU can report this event via DID “Reset Request: I2C Slave Micro”

The host microprocessor shall implement a counter to keep count of this event.

This event can be reported via DTC “Multiple reset requests received” if there are greater than 5 reset requests during any single ignition cycle.

Loss of communication

DL\_FPD LINK\_REQ\_\_3.4.3.5

During normal operation, the host microprocessor shall determine loss-of-communication by monitoring for I2C NAK response.

If the host microprocessor detects a condition where the LVDS link is operational but the remote node detects an intermittent NAK the host microprocessor will retry I2C transmission.

If the host microprocessor detects a condition where the LVDS link is operational but the local/remote node detects a persistent NAK response (> 500ms) to a peripheral device, the host ECU shall have ability to set DTC “Lost Communication” with appropriate peripheral device connected to the local/remote node.

## Remote Node Requirements

An FPD LINK remote node communicates to a local node, and optionally one or more remote nodes. A remote node cannot independently send data to other remote nodes. The local node shall be the source of data to all remote nodes.

### Remote Node Initialization

DL\_FPD LINK\_REQ\_\_

Once the local node is setup according to REQ\_\_3.3.1.1 registers present in the remote node specified in table 6a and 6b shall be read and values updated if required.

### Remote Node Status

DL\_FPD LINK\_REQ\_\_

All remote nodes have capability to detect FPD LINK Bit/Data errors.

The host microprocessor shall monitor appropriate registers specified in Table 8a, 8b, 9a and 9b and report errors as well as maintain error counters as specified in REQ\_\_3.3.2.3

In case of loss of lock remote register status may not be available.

Peripherals error reporting

DL\_FPD LINK\_REQ\_\_

Remote node may detect errors related to the peripherals attached to it, and may report this information via FPD LINK (via the slave interrupt), and/or using CAN. Remote node shall **NOT REPORT** peripheral errors using the **FPD LINK** Network Error DTC (slaves should use a Video System specific DTC).

### Remote Node Error recovery

DL\_FPD LINK\_REQ\_\_

Remote node does not handle error recovery. The local node is responsible for monitoring link status and error recovery.

# VERIFICATION METHODS

## Node conformance tests

All FPD LINK network nodes must demonstrate conformance to the applicable tests defined in the conformance tests in table below.

|  |  |
| --- | --- |
| **Protocol** | **Conformance test** |
| FPD LinkPhysical Layer Design Verification Checklist 00.06.03.401 | Ref [5] |
| FPD LinkImplementation Review Checklist 00.06.01.405 | Ref [6] |
| FPD Link III System Level Design Verification Checklist 00.06.01.404 |  |

## Verification traceability

The following matrix itemizes all requirements specified herein and cross-references them to one of several means for verification. Due the criticality of a requirement there may be more than one procedure identified for verification. Below is a brief description of each of the verification methods:

ECU Level Test Plans Design Verification test where requirements are verified on a specific ECU.

Vehicle Level Test Plans Design Verification test where requirements are verified at a Vehicle Level.

Hardware Review Inspection Inspection where requirements are verified during a Hardware Review. Reference [5], [6].

Application Testing Testing performed on the application software, by (sub)system engineering group which verifies the requirement.

| **Requirement No.** | **Vehicle Level DV (System)** | **Implementation Level Review** |
| --- | --- | --- |
| Maximum Clock Rate  DL\_FPD LINK\_REQ\_\_3.1.1.1 | x | x |
| Forward Channel Data Rate  DL\_FPD LINK\_REQ\_\_3.1.2.1 | x | x |
| cable/connectors assemblies Selection  DL\_FPD LINK\_REQ\_\_3.1.2.2 | x | x |
| Back Channel Data Rate  DL\_FPD LINK\_REQ\_\_3.1.3.1 | x | x |
| Supported formats  DL\_FPD LINK\_REQ\_\_3.1.4.1 | x | x |
| Common FPD Link III Network Wakeup Source  DL\_FPD LINK\_REQ\_\_3.2.3.1 | x | x |
| Local Node Initialization  DL\_FPD LINK\_REQ\_\_3.3.1.1 |  | x |
| Chipset power-up sequence  DL\_FPD LINK\_REQ\_\_3.3.1.2 |  | x |
| Initialization Time  DL\_FPD LINK\_REQ\_\_3.3.1.3 |  | x |
| Video master clock  DL\_FPD LINK\_REQ\_\_3.3.1.4 | x | **x** |
| Software Driver  DL\_FPD LINK\_REQ\_\_3.3.1.5 |  | **x** |
| I2C Clock Stretching  DL\_FPD LINK\_REQ\_\_3.3.1.6 | x |  |
| GPIO state during loss of lock  DL\_FPD LINK\_REQ\_\_3.3.1.7 |  | x |
| Disabling unused channels on hubs  DL\_FPD LINK\_REQ\_\_3.3.1.8 |  | x |
| Auto equalization behavior  DL\_FPD LINK\_REQ\_\_3.3.2.1 | x | x |
| Loss of Lock Fault  DL\_FPD LINK\_REQ\_\_3.3.2.2 |  | x |
| Detection and reporting of FPD LINK III network errors  DL\_FPD LINK\_REQ\_\_3.3.2.3 |  | x |
| Error handling procedure  DL\_FPD LINK\_REQ\_\_3.3.3.1 |  | x |
| Remote node being unresponsive/offline  DL\_FPD LINK\_REQ\_\_3.3.3.2 |  | x |
| FPD Link III Network Discovery at EOL/Service Bay  DL\_FPD LINK\_REQ\_\_3.4.1.1 | x |  |
| FPD Link III Network Errors  DL\_FPD LINK\_REQ\_\_3.4.2.1 | x |  |
| Link Status  DL\_FPD LINK\_REQ\_\_3.4.3.1 | x | x |
| Lock Status  DL\_FPD LINK\_REQ\_\_3.4.3.2 |  | x |
| Unexpected Reset  DL\_FPD LINK\_REQ\_\_3.4.3.3 |  | x |
| Peripheral device reset request  DL\_FPD LINK\_REQ\_\_3.4.3.4 |  | x |
| Loss of communication  DL\_FPD LINK\_REQ\_\_3.4.3.5 |  | x |
| Remote Node Initialization  DL\_FPD LINK\_REQ\_\_3.5.1.1 |  | x |
| Remote Node Status  DL\_FPD LINK\_REQ\_\_3.5.2.1 |  | x |
| Peripherals error reporting  DL\_FPD LINK\_REQ\_\_3.5.2.2 |  | x |
| Remote Node Error recovery  DL\_FPD LINK\_REQ\_\_3.5.3.1 |  | x |



# Appendixes

## Appendix. 1 Approved FPD LINK Chipsets

Approval of FPD LINK chipsets will be addressed by the Advanced Netcom. The current approved list of chipsets are specified in FPD LINK III Approved Chipsets [2].

**Note:** Some chipsets that haven’t been approved such as DS90UB914A and DS90UB934 have been mentioned in this document because they are being used in current production vehicles. The chipsets that aren’t approved aren’t recommended for use in any new programs. For latest list please refer FPD LINK III Approved Chipsets document.

## Appendix. 2 DTC/DID list

|  |  |  |
| --- | --- | --- |
| DTC | Condition | Type |
| Loss of lock | Set when five (5) instances of Loss of Lock occur within a key cycle. | Required |
| Unable to configure FPD link | Set when unable to configure on startup, network has errors that result in a no configuration condition | Required |
| Unexpected Reset | Set when five (5) instances of Loss of Lock or Reset request occur within a key cycle. | Optional |
| LVDS Link Fault | Set when Loss of Communication with I2C Slave Microcontroller | Required |
| LVDS General Electric Failure | Set when the host microprocessor cannot communicate with the local node after power is being supplied to it | Required |
| Multiple Reset Request Received | Set when peripheral devices connected to the chipset requests for more than five (5) resets within a key cycle. | Optional |
| Loss Of Communication | Set when the host microprocessor detects a condition where the LVDS link is operational but the local/remote node has a persistent NAK response (> 500ms) from a peripheral device connected to it. | Required |

Table 11: DTC list

|  |  |  |
| --- | --- | --- |
| DID | Description | Type |
| Loss of Lock | Status of Loss of lock event | Required |
| Network Error | Keeps count of Network errors, will provide channel data integrity information | Optional |
| Transient Error | Keeps count of Transient errors, will show if any random errors occurred | Optional |
| Unexpected Reset | Keeps count of Unexpected resets | Optional |
| LVDS Link Fault | Keeps count of LVDS Link fault | Required |
| Reset Request | Updates if a peripheral requests a reset | Required |

Table 12: DID list

The DTC/DID names are only suggestive, appropriate names and numbers should be used according to the application the chipsets are used for with approval from Netcom.

## Appendix. 3 Change log

6/11/2018: Initial release.

1/2/2019: Update to include FPD link IV chipsets